IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 41. (Cancelled

42. (Currently Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions and a gate electrode between said first semiconductor regions;

second semiconductor regions arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET through one of said first conductor plugs, wherein said first conductive strip is formed in a separate manufacturing step from said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second semiconductor regions through said first conductor plugs to electrically connect said second semiconductor regions to one another through said second conductive strip, wherein said second conductive strip is formed in a ~~separated~~separate manufacturing step from said first conductor plugs;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug,

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.

43. (Previously presented) A semiconductor integrated circuit device according to claim 42, wherein each of said first conductor plugs comprises a tungsten film.

44. (Previously presented) A semiconductor integrated circuit device according to claim 43, wherein each of said first conductor plugs comprises a multiplayer film of titanium nitride and tungsten.

45. (Previously Presented) A semiconductor integrated circuit device according to claim 43, wherein said second semiconductor regions comprise an n-type semiconductor region and a p-type semiconductor.

46. (Previously Presented) A semiconductor integrated circuit device according to claim 45, wherein said second conductor plug comprises a tungsten film.

47. (Previously Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions of n-type conductivity and a gate electrode between said first semiconductor regions;

a second semiconductor region of n-type conductivity and a third semiconductor region of p-type conductivity arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs each comprising a tungsten film formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET through one of said first conductor plugs, wherein said first conductive strip is formed in a separate manufacturing step from said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second and third semiconductor regions through said first conductor plugs to electrically connect said second and third semiconductor regions to one another through said second conductive strip, wherein said second conductive strip is formed in a separate manufacturing step from said first conductor plugs;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug,

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.

48. (Previously Presented) A semiconductor integrated circuit device according to claim 47, wherein each of said first conductor plugs comprises a multi-layer film of titanium nitride and tungsten.

49. (Previously Presented) A semiconductor integrated device according to claim 47, wherein said second conductor plug comprises a tungsten film.

50. (New) The semiconductor integrated device according to claim 42, further comprising:

first silicide layers formed between surfaces of said first semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said first semiconductor regions; and

second silicide layers formed between surfaces of said second semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said second semiconductor regions.

51. (New) The semiconductor device according to claim 47, further comprising:

first silicide layers formed between surfaces of said first semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said first semiconductor regions; and

second silicide layers formed between surfaces of said second semiconductor regions and said plurality of first conductor plugs formed in said openings in said first insulating film on said second semiconductor regions.

REMARKS

Reconsideration and allowance of this application is respectfully requested.

This amendment is in response to the Office Action dated June 30, 2003. By the present amendment, new claims 50 and 51 are presented to define further aspects of the present invention.

Reconsideration and removal of the rejection of claims 42-49 as being unpatentable over the combination of Wu (USP 4,859,619) in view Ho (USP 4,954,214), Tseng (USP 6,090,700) or Lee (USP 5,748,521) is respectfully requested for the reasons set forth below.

At the outset, it is noted that Applicants are submitting herewith a sworn translation of the Japanese priority document JPA 8-137957, filed on May 31, 1996, in order to overcome the use of the Lee patent (USP 5,748,521) as a reference in this case. With regard to this, it is noted that the Lee patent was filed in the United States on November 6, 1996, subsequent to the May 31, 1996 Japanese priority date to which the present application is entitled. Accordingly, the following discussion is premised on the fact that Lee is not available as prior art.

As discussed in the April 11, 2003 Amendment in this case, an important feature of the present invention is the use of conductor plugs in a semiconductor circuit having a first portion for a memory array and a second portion for a circuit other than a memory array. More specifically, as an example of this, reference is made to Fig. 9 of the present application in which first conductor plugs are shown with the numeral 23. These first conductor plugs 23 are filled into conductor holes such as shown in Fig. 8. Following this, as set forth in both independent claims 42 and 47, first and second conductive strips are respectively formed over the first

conductor plugs (as can be seen in Fig. 10). Thus, as specifically set forth in claims 42 and 47:

> "said first conductive strip is formed in a separate manufacturing step from said first conductor plugs; and
> ...said second conductive strip is formed in a separate manufacturing step from said first conduct plugs."

As further discussed in the previous amendment, the significance of using such plugs in the memory device is that the contact holes can be made smaller and the conductive layers can have a flat and even surface.

In the Office Action, it is recognized by the Examiner that the primary reference to Wu fails to teach or suggest the formation of first and second conductive strips in a separate manufacturing step from the formation of the first conductor plugs (e.g. see paragraph 3 of the Office Action). Indeed, as clearly illustrated in Fig. 7 of Wu, the Wu reference does not actually provide conductor plugs at all. Instead, metal layer such as shown by the numeral 81 are provided in Wu to fill contact holes 78 and provide upper regions for contacting upper layers such as 87. The problem with this one-step arrangement is the uneven upper surface for contact regions, as clearly shown in the indentations in the upper surface of the metal layer 81 in Fig. 7.

In the Office Action, it is stated in paragraph 3 that the shortcoming of the Wu reference in not teaching forming first and second conductive strips in a separate manufacturing step from first conductor plugs is overcome by the teachings of Lee and Tseng. As noted above, the Lee patent is unavailable as a reference since its filing date is subsequent to the priority date to which the present application is entitled under 35 U.S.C. § 119. With regard to the Tseng patent, although this represents a generalized teaching of forming metal contacts such as identified by the numeral 34 over plugs identified by the numeral 38, there is nothing in this

reference to indicate that these teachings would be useful in a memory array. With regard to this, it is noted that memory arrays are formed with processes different than those used in other types of integrated circuits due to various restrictions which exist in the construction of memory arrays. As such, it is not common to use conductor plugs in memory arrays, and certainly is not a matter of design choice to do so. As such, it is respectfully submitted that there is no motivation whatsoever, other than the Applicants' own teachings, for utilizing the arrangement taught by Tseng, which make no mention whatsoever of use of his teachings in memory arrays, to modify the Wu reference to arrive at the present claimed invention. As noted above, Wu simply provides a one piece structure such as shown with the metalization 81, and gives no suggestion of modifying this. Tseng teaches nothing with regard to memory arrays, and certainly does not make any suggestion for overcoming a problem such as the indentations formed in the upper surface of the metalizations 81 of Wu. As such, it is respectfully submitted that the only motivation for such a modification of Wu would be Applicants' own teachings, the use of which is, of course, improper in formulating a rejection.

With regard to this, attention is addressed to the recent decision of the CAFC in the matter of *In re* Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002). As set forth in that case:

> "With respect to Lee's application, neither the Examiner nor the Board adequately supported the selection and combination of the Nortrup and Thunderchopper references to render obvious that which Lee described. The Examiner's conclusuary statements ...do not adequately address the issue of motivation to combine. This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been lead to this combination of references, simply to "use that which the inventor taught against its teacher." 61 USPQ 2d @ 1434 (underlining added)

In the present case, it is respectfully submitted that essentially the same situation exists. Other than Applicants' own teachings, there is nothing that would have lead one of ordinary skill in the art "to this combination of references." As noted above, Tseng has nothing whatsoever to do with memory arrays or forming conductor plugs or conductive layers for such memory arrays. As also noted above, it is not at all common to use such conductor plugs for memory arrays. Therefore, it is urged that this combination of references is improper for the reasons set forth in the case of *In re* Lee, and reconsideration and removal of the rejection based on the combination of Wu and Tseng is earnestly solicited.

Similarly, as discussed in the preceding Amendment filed on April 11, 2003 in this case, nothing in the Ho reference would suggest modification of Wu to arrive at the claimed invention either. Like Tseng, Ho fails to teach or suggest anything with regard to using conductor plugs and separate conductive layers in a memory array arrangement. On the contrary, the Ho reference is directed to CMOS devices and give no suggestion at all for using such conductor plugs with separately formed conductive layers in a first portion having a memory array and a second portion for a circuit other than a memory array. Accordingly, the same points noted above concerning the case of *In re* Lee apply to the combination of Wu and Ho since neither of these references provides the necessary motivation for the combination proposed in the Office Action. Therefore, again, reconsideration and allowance of the pending claims over this combination of references to Wu and Ho is respectfully requested.

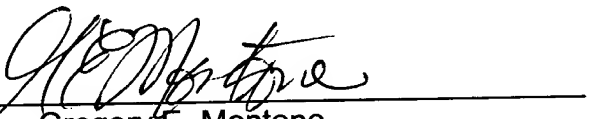
For the reasons set forth above it is respectfully submitted that claims 42-49 and newly presented claims 50 and 51 patentably define over the cited prior art, and reconsideration and allowance of these claims is earnestly solicited.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.35437CV2), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 

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